Soitec and PSMC collaborate on ultra-thin TLT technology for nm-scale 3D stacking

Bernin (France), June 3, 2025 – Soitec (Euronext – Tech Leaders), a world leader in the design and production of innovative semiconductor materials, today announced a strategic collaboration with Powerchip Semiconductor Manufacturing Corporation (PSMC).

Under the collaboration, Soitec will supply PSMC 300mm substrates incorporating a release layer, Transistor Layer Transfer (TLT) ready, to support a new demonstration of advanced 3D chip stacking at the wafer level. This marks the first public announcement of Soitec's TLT technology.

The technology is an enabler for next-generation semiconductor designs that allow for more powerful, compact and energy-efficient chips – with potential applications ranging from smartphones, tablets and AI devices to autonomous driving systems.

Soitec's Chief Technology Officer and Senior EVP Innovation, Christophe Maleville said: "*At Soitec we are proud to pioneer semiconductor materials that unlock new possibilities in chip design and performance. Our collaboration with PSMC reflects a shared commitment to pushing the boundaries of 3D integration and supporting the global shift toward more efficient and compact computing architectures. Together we are laying the groundwork for the next generation of semiconductor innovation*."

PSMC Chief Technology Officer SZ Chang said: *"With our longstanding presence in memory and logic foundry, PSMC consistently drives advancements in 3D stacking. In the two-year collaboration, PSMC has demonstrated an innovative wafer-stack integrated process by leveraging Soitec's advanced substrate technology. The innovation significantly broadens the 3D technology from chip-level stacking - optimizing power performance in computing architecture, to transistor-level stacking – extending Moore's law, with a remarkable reduction in stacking wafer thickness from micrometer to nanometer level. This achievement, by pushing the boundaries of 3D stacking, reaffirms our position at the forefront of the semiconductor industry."*

To meet growing industry demand for faster and more energy-efficient chips, Soitec has developed a new substrate stack enabling high-speed transfer of ultra-thin transistor layers onto different types of wafers—a key requirement in heterogeneous integration, where diverse chip components are combined in a single package.

The stacking process enables multiple transistor layers to be built vertically to support 3D transistor architectures including vertical field-effect transistors (FETs) with backside power delivery networks (PDNs).

This TLT substrate leverages Smart Cut™ technology together with infrared (IR) laser release processing. The proprietary Soitec technology enables the formation of an ultra-thin semiconductor layer, ranging from 5nm to 1µm in thickness, on top of the TLT substrate. Once devices are fabricated on the TLT wafer, the IR laser process facilitates the lift-off of the ultra-thin

layer from the substrate to the target wafer, without introducing thermal stress or damaging the devices.

The Soitec-PSMC collaboration builds on existing France-Taiwan cooperation initiatives in AI and other semiconductor-related domains.

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About Soitec

Soitec (Euronext - Tech Leaders), a world leader in innovative semiconductor materials, has been developing cutting-edge products delivering both technological performance and energy efficiency for over 30 years. From its global headquarters in France, Soitec is expanding internationally with its unique solutions, and generated sales of 0.9 billion Euros in fiscal year 2024-2025. Soitec occupies a key position in the semiconductor value chain, serving three main strategic markets: Mobile Communications, Automotive and Industrial, and Edge and Cloud AI. The company relies on the talent and diversity of its 2,300 employees, representing 50 different nationalities, working at its sites in Europe, the United States and Asia. Soitec has registered over 4,000 patents.

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About Powerchip Semiconductor Manufacturing Corporation (PSMC)

Powerchip Semiconductor Manufacturing Corporation (PSMC) is the world's seventh-largest pure-play foundry, with four 12-inch and two 8-inch fabs in Taiwan, capable of producing over 2.1 million 12-inch equivalent wafers annually. Since its establishment in 1994, the company transitioned successfully from DRAM manufacturing to advanced foundry services for memory and logic chips. Ranked seventh in global semiconductor ESG evaluations, PSMC demonstrates strong governance and environmental commitment. In May 2024, PSMC's new 12-inch fab in Taiwan's Tongluo Science Park began operations with a planned capacity of 1.2 million wafers annually, using advanced 28nm and wafer stacking technologies.

For more information, visit https://www.powerchip.com/en-global